CLAIMS

What is claimed is:

1. A circuit comprising:

   a signal trace to receive a first large signal;

   a first plurality of signal traces to receive a small signal pair;

   a clock trace to receive a clock signal; and

   a mixed signal circuit having at least a first and a second element, coupled to the signal trace, the first plurality of signal traces and the clock trace, to facilitate generation of a second large signal based at least in part on the small signal pair and the first large signal, with the first large signal and the clock signal driving the first and second elements respectively to transition asynchronously.

2. The circuit of claim 1 wherein the mixed signal circuit comprises a pull-down network.

3. The circuit of claim 2 wherein the pull-down network comprises an AND stack.

4. The circuit of claim 3 wherein an internal node of the AND stack is precharged and pre-discharged by the first large signal.

5. The circuit of claim 1 wherein the mixed signal circuit comprises precharge circuitry coupled to the second large signal trace, a third large signal trace

and the clock trace to precharge the second large signal trace and the third large signal trace to a first voltage level.

6. The circuit of claim 5 further comprising sample circuitry coupled to the second and the third large signal traces to facilitate detection of a transition on one of the second and the third signal traces from the first voltage level to a second voltage level, sample circuitry to reinforce the second voltage level on the signal trace detected in transition and to assert the first voltage level on the signal trace not detected in transition.

7. The circuit of claim 6 wherein said sample circuitry comprises cross coupled P-MOSFET devices.

8. The circuit of claim 1 further comprising

a second plurality of signal traces to receive a small signal differential pair; and

a sense amplifier coupled to the second plurality of signal traces to receive a small signal differential pair and coupled to the first plurality of signal traces to provide the small signal pair.

9. The circuit of claim 7 wherein the sense amplifier precharges the small signal pair to a low value during an inactive phase of the clock signal.

10. The circuit of claim 7 wherein the sense amplifier comprises a ratioed P sense amplifier.

11. A circuit comprising:

a first signal trace to receive a first large signal;

a first plurality of small signal traces to receive a small signal pair;

a mixed signal circuit coupled to the signal trace and one of the first plurality of small signal traces to facilitate generation of a second large signal on a second signal trace wherein the second large comprises a logic value of a logic function of one small signal of the small signal pair corresponding to the one of the first plurality of signal traces and the first large signal, wherein the first large signal transitions asynchronously to a clock signal.

12. The circuit of claim 11 wherein the mixed signal circuit comprises an AND stack.

13. The circuit of claim 12 wherein an internal node of the AND stack is precharged by the first large signal.

14. The circuit of claim 11 wherein the mixed signal circuit comprises precharge circuitry coupled to the second large signal trace, a third large signal trace

and the clock trace to precharge the second large signal trace and the third large signal trace to a first voltage level.

15. The circuit of claim 14 further comprising sample circuitry coupled to the second and the third large signal traces to facilitate detection of a transition on one of the second and the third signal traces from the first voltage level to a second voltage level, sample circuitry to reinforce the second voltage level on the signal trace detected in transition and to assert the first voltage level on the signal trace not detected in transition.

16. The circuit of claim 15 wherein said sample circuitry comprises cross coupled P-MOSFET devices.

17. The circuit of claim 11 further comprising:

a second plurality of signal traces to receive a small signal differential pair; and

a sense amplifier coupled to the second plurality of signal traces to receive a small signal differential pair and coupled to the first plurality of signal traces to provide the small signal pair.

18. The circuit of claim 17 wherein the sense amplifier precharges the small signal pair to a low value during an inactive phase of the clock signal.

19. The circuit of claim 11 wherein the logic function comprises one of an NAND, NOR, multiplexor and exclusive-NOR.

20. A system comprising:

a processor including;

a circuit comprising:

a signal trace to receive a first large signal;

a first plurality of signal traces to receive a small signal pair;

a clock trace to receive a clock signal; and

a mixed signal circuit having at least a first and a second element, coupled to the signal trace, the first plurality of signal traces and the clock trace, to facilitate generation of a second large signal based at least in part on the small signal pair and the first large signal, with the first large signal and the clock signal driving the first and second elements respectively to transition asynchronously;

a networking interface;

a memory configured to store data; and

a bus coupled to the processor, networking interface and memory.

21. The system of claim 20 wherein the mixed signal circuit comprises a pull-down network implementing a logic function between the first large signal and the logic value associated with the small signal pair.

22. The system of claim 21 wherein the pull-down network comprises an AND stack.

23. The system of claim 22 wherein an internal node of the AND stack is precharged/pre-discharged by the first large signal.

24. The system of claim 20 wherein the mixed signal circuit comprises precharge circuitry coupled to the second large signal trace, a third large signal trace and the clock trace to precharge the second large signal trace and the third large signal trace to a first voltage level.

25. The system of claim 24 further comprising sample circuitry coupled to the second and the third large signal traces to facilitate detection of a transition on one of the second and the third signal traces from the first voltage level to a second voltage level, sample circuitry to reinforce the second voltage level on the signal trace detected in transition and to assert the first voltage level on the signal trace not detected in transition.

26. The system of claim 20 wherein the circuit further comprises:

a second plurality of signal traces to receive a small signal differential pair; and

a sense amplifier coupled to the second plurality of signal traces to receive a small signal differential pair and coupled to the first plurality of signal traces to provide a small signal pair.

27. The system of claim 26 wherein the sense amplifier comprises a ratioed P sense amplifier.